AHB interface EMB

User Guide

03/2018

Hercules Microelectronics, Inc.
China

Contents

1 Introduction

This document mainly describes the usage of the AHB interface EMB IP. It works as AHB bus slave. So, it is used to facilitate user to connect EMB to AHB bus.

The AHB interface EMB IP supports the following features:

- Supports AHB interface protocols
- Supports single and burst operation
- Supports three EMB types : True Dual Port, Simple Dual Port and Single Port
- The interface type can be configured
- 32-bit AHB data buses
- EMB data width can be configured
- Address width can be configured
- Configurable memory initialization
- Base Address can be configured

Device family support:

HME-M7

2 AHB interface EMB Overview

2.1 Pin Description

Table 2-1 ***AHB interface EMB Pin description***

Interface		Name	Direction	Width	Description
AHB interface signal		hclk	Input	1	AHB interface clock
		hresetn	Input	1	AHB interface reset, low active
		haddr	Input	32	AHB address bus
		hwrite	Input	1	AHB transfer direction: 1-write, 0-read
		hwdata	Input	32	AHB write data bus
		hrdata	Output	32	AHB read data bus
		hsel	Input	1	AHB slave select signal
		hready_out	Output	1	Transfer done output
		hresp	Output	1	Transfer response signal
		htrans	Input	2	AHB Transfer type signal
		hsize	Input	3	AHB Transfer size
		hburst	Input	3	AHB Transfer type signal
EMB port	sp	clk	Output	1	Clock signal
		a	Output	4~19	Address signal
		d	Output	<= 32	Write data signal
		ce	Output	1	Select signal, high active
		we	Output	1	Data direction:1-write,0-read
		q	Input	<= 32	Read data signal
	tdp	clka	Output	1	Clock signal
		cea	Output	1	Select signal, high active
		wea	Output	1	Data direction:1-write,0-read
		aa	Output	4~19	Address signal
		da	Output	<= 32	Write data signal
		qa	Input	<= 32	Read data signal
	sdp	clkw	Output	1	Write clock signal
		cew	Output	1	Write select signal, high active
		aw	Output	4~19	Write address signal
		dw	Output	<= 32	Write data signal
		clkr	Output	1	Read clock signal
		cer	Output	1	Read select signal, high active
		ar	Output	4~19	Read address signal
		qr	Input	<= 32	Read data signal

2.2 Parameter Description

Table 2-2 ***AHB interface EMB parameter description***

Name	Type	Value	Description
START_ADDR	Integer	32'ha000_0000 ~32'hbfff_ffff Or 32'hc000_0000 ~32'hdfff_ffff	Base Address access the EMB,1K boundary，varies EMB depth.
EMB_TYPE	Integer	01/10/11	EMB work mode:01-sp,10-sdp,11-tdp
ADDRESS_WIDTH	Integer	4~19	Address width for EMB with sp mode
DATA_WIDTH	Integer	<= 32	Data width for EMB with sp mode
WR_PORT_TYPE	Integer	0/1	Write port interface type for EMB with sdp mode
RD_PORT_TYPE	Integer	0/1	Read port interface type for EMB with sdp mode
WR_ADDR_WIDTH	Integer	4~19	Write port address width for EMB with sdp mode
WR_DATA_WIDTH	Integer	<= 32	Write port data width for EMB with sdp mode
RD_ADDR_WIDTH	Integer	4~19	Read port address width for EMB with sdp mode
RD_DATA_WIDTH	Integer	<= 32	Read port data width for EMB with sdp mode
PORTA_ADDR_WIDTH	Integer	4~19	Port A address width for EMB with tdp mode
PORTA_DATA_WIDTH	Integer	<= 32	Port A data width for EMB with tdp mode

2.3 Block Diagram

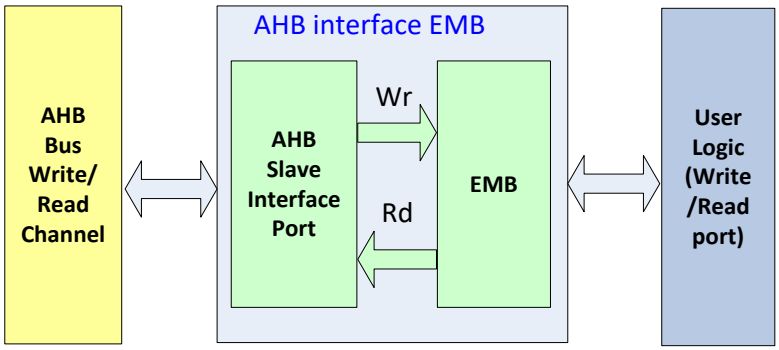

Figure 2-1(a) ***two types of interface EMB block diagram***

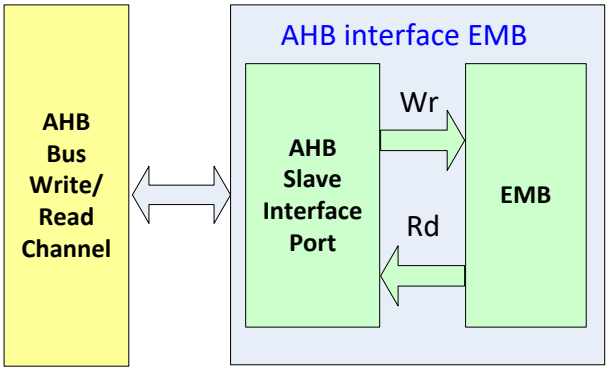

Figure 2-1(b) ***AHB interface EMB block diagram***

If the EMB works in the Single Port mode, then it only has the AHB slave interface. If the EMB works in the True Dual Port mode, its port A has AHB slave interface and port B is accessed by FPGA logic. If the EMB type is Single Dual Port, which port is of AHB interface can be configured.

3 AHB interface EMB IP Usage

3.1 AHB interface EMB operation timing diagram

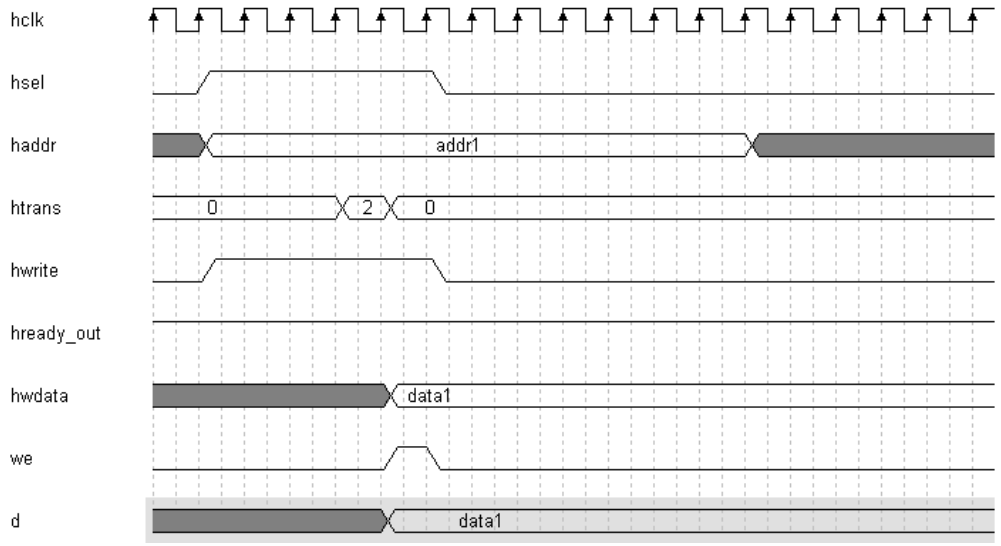

Figure 3-1 ***Basic write transfer***

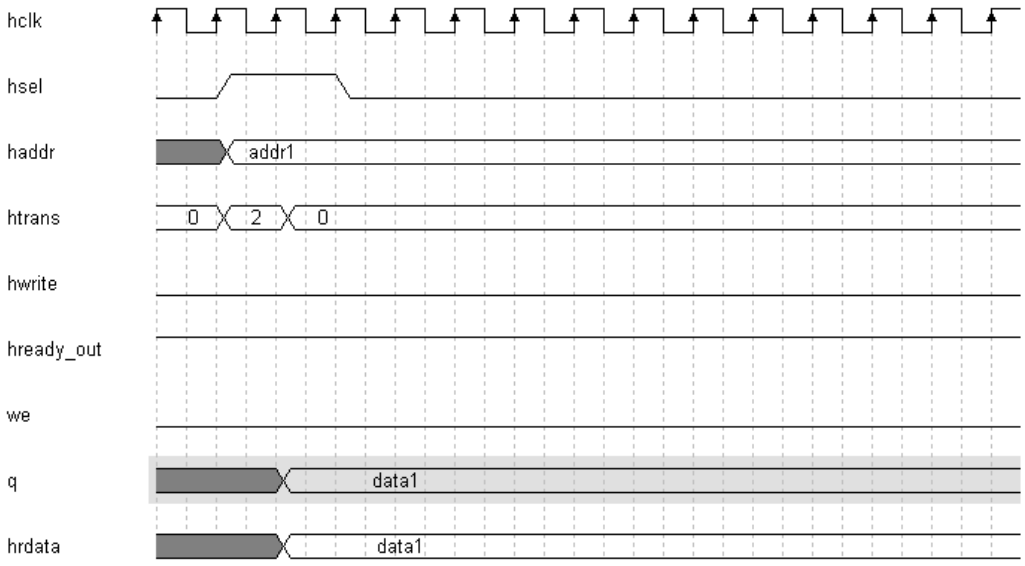

Figure 3-2 ***Basic read transfer***

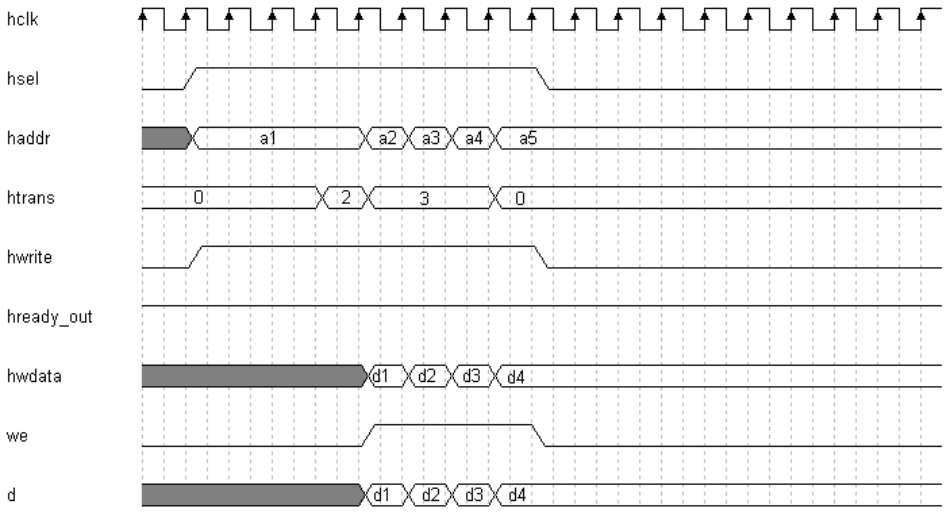

Figure 3-3 ***Burst write transfer***

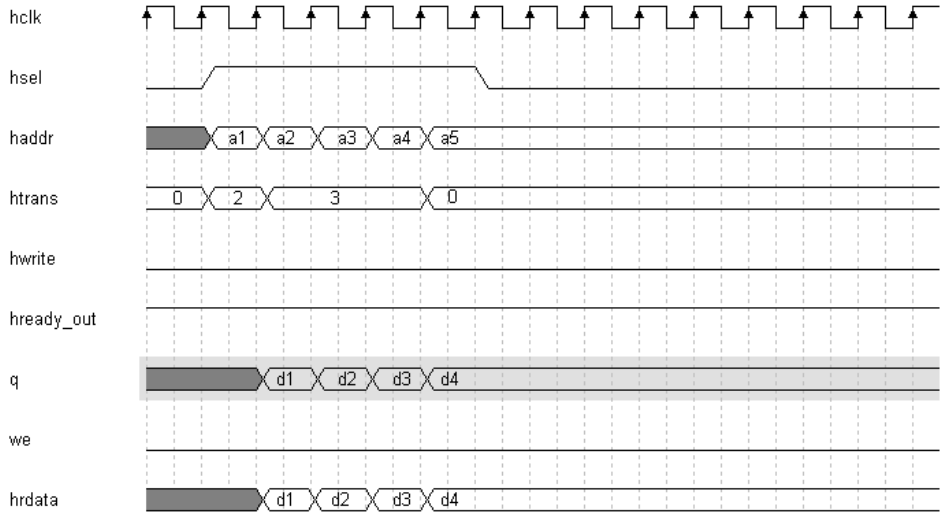

Figure 3-4 ***Burst read transfer***

In the figure 3-1, it is described how to transform the AHB bus signals to make them fit the EMB write operation .The single transfer consists of one address cycle and one data cycle on the AHB bus side.

When the trans signal is valid, the haddr and other control signals can be sampled and broadcasted to EMB on the next hclk rising edge.

In the figure 3-2, it is described how to transform the AHB bus signals to make them fit the EMB read operation .The single transfer consists of one address cycle and one data cycle on the AHB bus side.

When the trans signal is valid, the haddr and other control signals can be sampled and broadcasted to EMB on the next hclk rising edge. The read data from EMB are routed directly back to the AHB.

3.2 AHB interface EMB address mapping

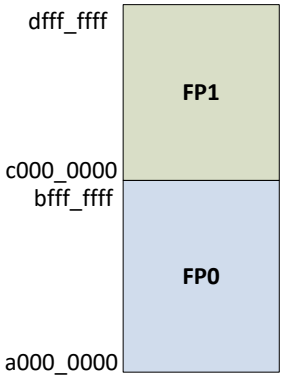

Figure 3-5 ***Address mapping***

The ARM Core provides two groups of AHB Bus signals, AHB0 and AHB1, so there are two memory space for user logic which are called as FP0 and FP1.It means that if you instantiate an ARM Core and choose the AHB0 , you must access your slaves on the address from a000_0000 to bfff_ffff, but if you connect the AHB interface EMB to AHB1, the slaves can be accessed on the address from c000_0000 to dfff_ffff.
The Base Address can be configured by user, 1K boundary.

4 Resource usage

Resource usage of the AHB interface EMB IP on Fuxi

Table 4-1 ***AHB interface EMB IP resource usage***

Resource	DepthxWidth	LUTs	Regs
Sp mode, use EMB5K	512x32	22	11
Sdp mode, write port is AHB interface, read port connect with FP logic, use EMB5K	512x32	11	11
Sdp mode, read port is AHB interface, write port connect with FP logic, use EMB5K	512x32	18	1
Tdp mode, port A is AHB interface, use EMB5K	512x32	22	11

5 Generate File Directory Structure

The AHB interface EMB IP wizard generated file includes: source files (src), simulation files (sim) and example design files and related document. The detailed design directory structure is as below.

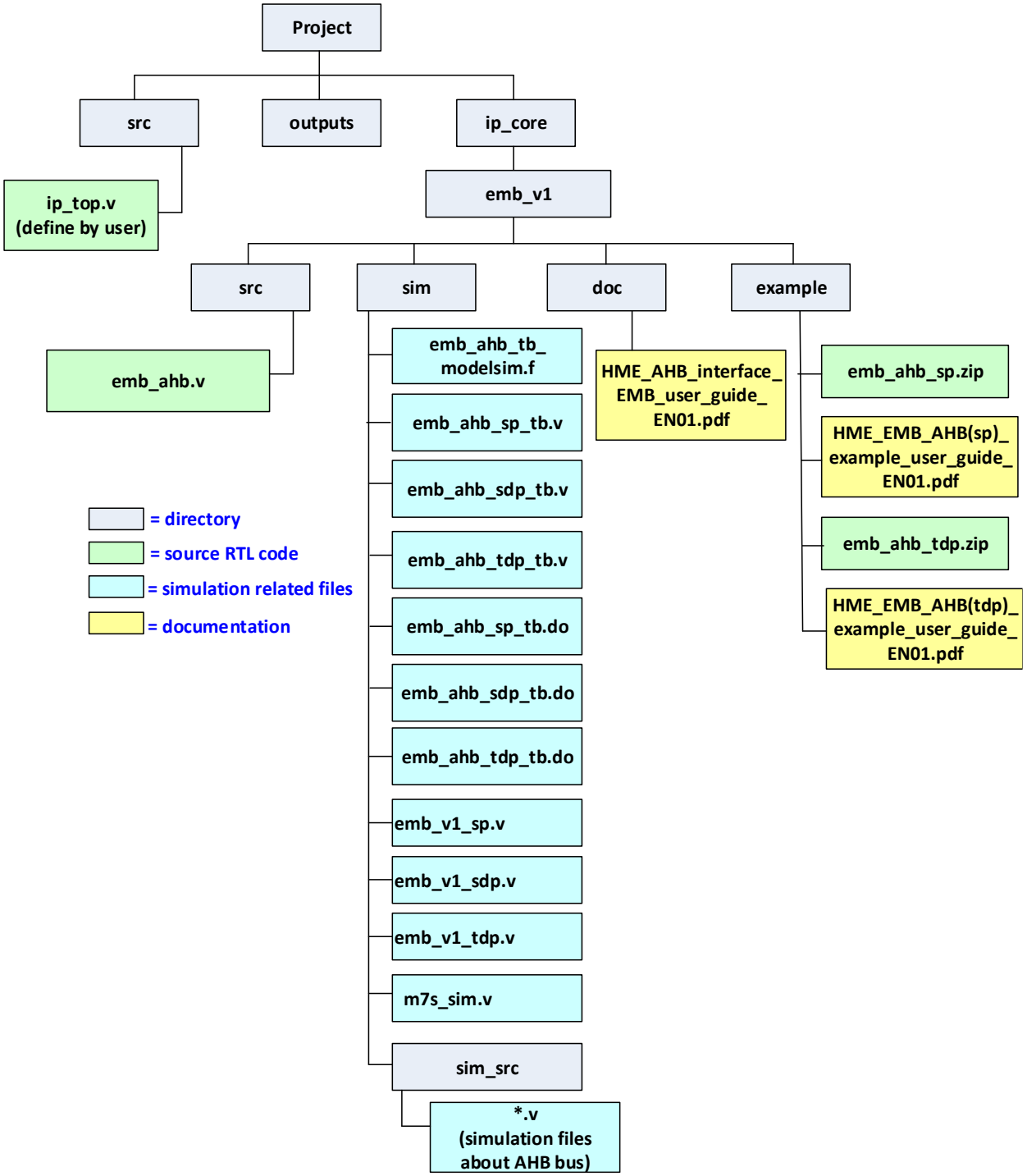

Figure 5-1 ***IP wizard generated file directory structure***

Table 5-1 ***Generated File Directory structure***

Directory	Description
src\	Directory for project source code, including IP wizard generate code.
ip_core\	The directory specially for all IPs
\emb_v1	Directory for ahb interface emb IP
\doc\HME_AHB_interface_EMB_user_guide_EN01.doc	User guide for ahb interface emb IP
\src	IP Design RTL
\src\emb_ahb.v	The src of ahb interface emb IP
\sim	
\ emb_ahb_sp_tb.v	Testbench of ahb interface emb(sp) IP
\emb_ahb_sdp_tb.v	Testbench of ahb interface emb(sdp) IP
\emb_ahb_tdp_tb.v	Testbench of ahb interface emb(tdp) IP
\ emb_ahb_sp_tb.do	Do script for Modelsim simulation (sp mode)
\ emb_ahb_sdp_tb.do	Do script for Modelsim simulation (sdp mode)
\ emb_ahb_tdp_tb.do	Do script for Modelsim simulation (tdp mode)
\emb_ahb_tb_modelsim.f	Modelsim simulation related files
\emb_v1_sp.v	Other RTL design files for simulation
\emb_v1_sdp.v	
\emb_v1_tdp.v	
\m7s_sim.v	
\sim_src	
*.v	Simulation files about AHB bus
\example	
emb_ahb_sp.zip	AHB interface emb IP example with sp mode
emb_ahb_tdp.zip	AHB interface emb IP example with tdp mode
HME_EMB_AHB(sp)_example_user_guide_EN01.pdf	The guide of ahb interface emb with sp mode
HME_EMB_AHB(tdp)_example_user_guide_EN01.pdf	The guide of ahb interface emb with tdp mode

Revision History

Revision	Date	Comments
1.0	2018-03-26	Initial release